ABSTRACT
The fabrication of WOW (wafer-on-a-wafer) with MEMS technology has been developed. A wafer was thinned and stacked on a base wafer. After the TSVs were patterned on the thinned wafer, they were filled by Cu for interconnection. The wafers were bonded with benzocyclobutene (BCB, CYCLOTENE™) as an adhesive material. The BCB layer was also acted as a dielectric layer between top and bottom silicon wafers. The TSVs were created by DRIE (Deep Reactive Ion Etching) and filled by Cu electroplating. This paper describes that thinned Si wafers down to 20µm were stacked on a base wafer with TSVs interconnection filled by Cu. The thinned wafers were stacked up to seven. The electrical characteristics were measured by daisy-pattern including 243 TSVs filled by Cu and the stress simulation for TSV was also shown.

KEYWORDS
WoW, BCB, CYCLOTENE, TSV, Cu interconnection, wafer-level packaging, stacking.

INTRODUCTION
In recent years, the scale of semiconductor devices comes to the limit in the points of lithography, heat value, and so on. Three-dimensional interconnection by TSV between semiconductor devices is expected to solve these issues. The TSV interconnection filled by Cu has been researched and reported in published papers [1-5]. However, the TSV technology is still on the stage of research and has many points to improve in the view of fabrication processes.

The key issues for three-dimensional interconnection are 1) stacking on wafer level, 2) TSVs with low aspect ratio, 3) via last formation, and 4) bump-less contact. The conventional stacking methods are chip to chip or wafer to wafer stacking. These methods have disadvantages for through-put and process cost. Therefore, wafer-level stacking has to be required. The 2) low aspect ratio of TSVs reduces process difficulty and leads to short process time and high yield rate. The 3) via-last formation decreases fabrication damage for the semiconductor devices. Finally, the 4) bump-less contact removes the problems of bump contact, for instance, tilting of the stacked chip, voids and so on.

This paper shows the solution for the issues mentioned above. The wafers were stacked on wafer-level with an adhesive layer of benzocyclobutene (BCB, CYCLOTENE™). The stacking with the BCB makes it possible to bump-less contact. The stacked Si wafers on a base wafer were thinned by back-grind to reduce the aspect ratio of TSVs. By repeating all the same processes for stacking and TSV formation filled by Cu, the several thinned wafers were stacked and interconnected with the base wafer, leading to high-density 3D packaging.

The mask design includes daisy-chain patterns on an 8inch wafer as shown in Figure1. The three dimensional interconnection technology has been developed for semiconductor devices mainly, however, the technology is very important for MEMS products as well. The electrical interconnection between MEMS devices and their package often results in making chip size large. Therefore, the stacking method with the BCB on wafer level and interconnection by Cu filled TSV meet the requirements for MEMS products and offers flexible packaging method with process compatibility of MEMS.

DESIGN AND FABRICATION PROCESS
Figure2 shows the process flow. A wafer, which was patterned by Au/TiN/Ti pads on SiN/SiO2 dielectric layers, was temporarily bonded to a glass wafer. The thickness of these layers was 130nm for Au, 50nm for Ti and TiN. The pattern size of the Au/TiN/Ti layer was 62µm long and
62μm wide. The thicknesses of the SiN and SiO2 layers were 200nm and 500nm respectively. The SiO2 layer was thermally oxidized and the SiN layer was deposited by LP-CVD (Low Pressure Chemical Vapor Deposition).

The patterned wafer was thinned down to 20μm thickness by back grind in DISCO corporation. The thinning process is shown in Figure3. The thinned wafer was stacked on a base wafer with an adhesive layer of BCB [6]. The thickness of the BCB layer was approximately 5 μm. Therefore, the total thickness of one layer was 25μm including the thinned Si and the BCB layer. The base wafer was also patterned by the same processes as the thinned wafer without the back grind and the temporary bonding. The pattern of the base wafer was 142μm long and 62μm wide of the Au/TiN/Ti pad. The thinned wafer was aligned with the base wafer with both-side alignment. After the glass is separated by wet process, photo-resist for the TSV layout with daisy chain was patterned on surface of the bonded wafer.

A. Back Grind

B. BCB Bonding

C. TSV

D. Side-wall Dielectric film

E. Cu Electroplating & Surface Planarization

The Au/TiN/Ti and SiN/SiO2 layers were etched by wet process and by RIE (Reactive Ion Etching), respectively. The silicon layer was processed by DRIE for TSVs (shown in Figure4) with small scallops of 100nm P-V. The diameter of the TSV holes was 30μm. After the BCB layer was etched by RIE with oxygen plasma [7], a dielectric layer of SiN with 1μm thickness was deposited by PE-CVD (Plasma Enhanced Chemical Vapor Deposition). The SiN layer was etched by anisotropic RIE without any masks, remaining the dielectric layer on the side wall and removing the top and the bottom, as shown in Figure5. Following the sputtering of a seed layer (Cu: 500nm, TiN: 50nm, Ti: 50nm), dry film resist (DFR) was patterned and the TSVs were filled by Cu electroplating. The top of Cu on TSVs was flattened by Surface planarTM of DISCO Corporation in Figure6.
Finally, the DFR was removed by wet process. By repeating the same process, several layers were stacked on top of the base wafer. It was demonstrated that total seven thinned wafers were stacked with Cu interconnections filled in TSVs (Figure7). After stacking several thinned Si with the BCB, the top side was patterned with photo-resist, following Ni and Au electroplating. The Au/Ni pads were acted as top electrodes for the daisy chain. The thicknesses of the Ni and Au were 1μm and 0.5μm respectively.

The resistance distribution of the daisy chain with 243 TSVs was measured after pad metal formation (Figure9). The medium value was the single TSV was 0.2 ohm, which almost corresponds to the theoretical value. It was demonstrated that the top and the bottom wafers were well-connected by the TSVs filled with Cu.

RESULTS AND DISCUSSIONS

The fabricated TSVs filled by Cu of 2 wafers stacked on the base wafer are shown in Figure 8. It was shown that the TSVs were filled by Cu and interconnected between top and bottom Si wafers without the voids. There were also no voids in the BCB layer between the thinned Si layers. It is turned out that the BCB is applicable for wafer bond. It is well-known that BCB has advantages of low-temperature curing, flatness, and the low dielectric constant. Therefore, BCB layer works well for not only dielectrics but also permanent adhesive bond.

The X-ray CT image is also shown in Figure 8. It was indicated that TSVs were filled by Cu uniformly.
The result of stress simulation is shown in Figure10. The simulation shows the stress comparison between the thick and thinned wafers. The result indicated that the thinned wafer suffered lower stress than the thick. Therefore, the thin wafer is suitable for stacking with Cu TSV interconnection comparing with the thick.

CONCLUSION
The TSVs interconnection on WOW was developed with MEMS technology. Several wafers up to seven were stacked with BCB. The electrical characteristics were measured and its result was appropriate. It was demonstrated of the bump-less stacking on wafer level and TVS interconnections filled by Cu. The process shown in the paper is so useful that it is applicable to various MEMS applications like μTAS, sensors, RF and so on. They are often required to seal in vacuum and interconnect between inner pads and outer pads. In addition, the size for packaging has to be as small as possible. The key technologies for small packaging are handling for thinner wafer and wafer-level bonding with metal interconnections of bump-less. The solution for the key technologies was shown in the paper. In the future, the vacuum seal by BCB will be researched and reported.

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