Impacts of Thermo-Mechanical Stresses on Bumpless Chip in Stacked Wafer Structure

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WOW: Wafer on Wafer
COW: Chip on Wafer
TSV: On-Chip-Via

FEA of 3 Stacked TSV
Maeda, et al. AMC2008

Kitada, et al. IITC2009

Bumpless Chip in Stacked Wafer Structure

Crack Issue in COW

COW Process Flow
Chip Bonding
Thinning
De-Bonding
Metallization

5 μm-thick Si COW
SEM Cross Sectional Image
Kelvin Via Resistance
Crack was observed after dicing

Material Properties

<table>
<thead>
<tr>
<th>Material</th>
<th>Young's Modulus (MPa)</th>
<th>Poisson's Ratio (v)</th>
<th>CTE (ppm K⁻¹)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>130000 @ 25°C</td>
<td>0.28</td>
<td>26 @ 25°C</td>
</tr>
<tr>
<td>BCB resin</td>
<td>2900 @ 25°C</td>
<td>0.32</td>
<td>42 @ 25°C</td>
</tr>
<tr>
<td>Epoxy resin</td>
<td>1000 @ 25°C</td>
<td>0.3</td>
<td>161 @ 150°C</td>
</tr>
</tbody>
</table>

Calculation Temperature 25°C – 25°C for BCB
5 @ 150°C for Epoxy

Summary

Impacts of Si thickness on the stresses in dielectric polymer for COW structure were investigated for the first time.
- Cracks are generated in high modulus dielectric polymer when Si thickness is 20 μm, where the FEA demonstrates high stresses in this structure.
- ERR shows that the crack propagates toward Si chip corner, then progresses at the interface of polymer and Si.
- On the COW structure, thinner Si chip and lower modulus polymer expand the process window.

Acknowledgement
Part of this work was implemented under the WOW alliance and the WOW Research Center Corporation.