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Abstract
Via-hole etching process with fine profile on Chip-on-Wafer (COW) stacking structure using bump-less off-chip-via interconnects was developed. Chips were arrayed and bonded on an 8-inch wafer. Gap between the chips was filled with dielectric polymer and the chips were thinned down to 5 μm by back grind process. Off-chip-vias were formed on dielectric polymer between chips. Copper redistribution line was formed with the semi-additive process. With the via thickness of 15 μm, the aspect ratio of via hole was 0.6 and no etching residues remained on the sidewall. No open failure on the contact resistance was measured and the medium value of via resistance was 0.18 ohm and 0.28 ohm at 25 μm and 10 μm diameter, respectively.

1. Introduction
3D-IC stacking is one of the most important key technologies for miniaturization and performance enhancement through the reduction of interconnect length in electronic systems. 3D technology has focused on production-worthy processing such as Chip-on-Wafer (COW) and Wafer-on-Wafer (WOW) because of productivity and costs as shown in Figure 1 [1, 2]. The COW stacking with off-chip-via has an advantage in utilizing conventional chips without modifying the chip layout for interconnection of TSV. Since the conventional COW process employs micro-bump and stack-last, bonding failure and chip destruction have arisen for the thinner chip stack. In our previous study, a stack-first and thinning-last COW processing using bump-less off-chip-via interconnects was revealed [3]. This paper reports on the development of dielectric polymer etching for off-chip-via.

2. Experimental
Figure 2 shows the COW process flow. Chips were bonded on an 8-inch glass substrate with a temporary adhesive. Non-conductive dielectric polymer was used to fill up the gap between the chips by squeegee process. After curing, the chips were thinned down to 5 μm from the backside. The chips were bonded on the other device wafer by permanent adhesive. A silicon dioxide layer of 1 μm was deposited by TEOS-based plasma enhanced chemical vapor deposition (PECVD) as a hard mask. Via-holes were formed at the off-chip area by dry etching. The barrier metal of Ti/TiN and seed-Cu were deposited by sputtering and via-holes were filled with Cu by electrochemical plating.

3. Results and Discussion
Total thickness variation of permanent adhesives was 0.5 μm (Figure 3). In this study, permanent adhesive was etched with O2/SF6 mixture gas by reactive ion etching (RIE). Permanent adhesive was loaded with 5% Si-filler powder, thus etching residue was remained under high pressure and low SF6 mixture ratio (Figure 4). It seems that low pressure and high SF6 mixture ratio lead to reduce etching residues on the sidewall.

Figure 5 shows the COW wafer after gap filling and thinning. There were center pad arrays for device connection and redistribution lines lead to off-chip-via. Figure 6 shows cross-sectional view of chip and off-chip-via. The chip thickness was 5 μm. The depth and the diameter of the off-chip-via were 15 μm and 25 μm respectively. Because the off-chip-via was formed at dielectric polymer, via capacitance was smaller than TSV formed at silicon substrate.

Figure 7 shows the electrical insulation property of redistribution lines. The result indicates isolation between adjacent lines and pads. Figure 8 shows the off-chip-via resistance with the thickness of 15 μm and 30 μm. With the via thickness of 15 μm, the medium value of via resistance was 0.18 ohm with 25 μm diameter and 0.28 ohm with 10 μm diameter. With the via thickness of 30 μm, the medium value of via resistance was 0.16 ohm with 25 μm diameter and 0.29 ohm with 10 μm diameter.

4. Conclusion
We fabricated a bump-less COW structure with off-chip-via. For the interlayer connection, via-holes were formed at the off-chip area by dry etching. By optimizing dry etch conditions, via-hole with fine profile and no etching residues on the sidewall was developed. No open failure on the contact resistance was measured.

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References
Figure 1. Comparison of cost efficiency as a function of production size.

Figure 2. Process flow of COW with off-chip-via.

Figure 3. Total thickness variation of permanent adhesive.

Figure 4. Cross-section view of off-chip-via.

Figure 5. Top view of COW with bump-less interconnects.

Figure 6. Cross-section view of chip and off-chip-via.

Figure 7. Leakage characteristic between redistribution lines.

Figure 8. Resistance of off-chip-via with via thickness of (a) 15 µm, (b) 30 µm.