Development of Multi-Stack Process on Wafer-on-Wafer (WOW)

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Abstract
The multi-stack process on wafer-on-wafer (WOW) has been developed. In order to realize the multi-stacked wafer with ultra thinned wafer of less than 10 μm with adhesive polymer, several processes have been optimized. The wafer thickness after back-grinding was controlled within the total thickness variation (TTV) of 1.2 μm on wafer-level of 8 inch. For the side wall of though silicon vias (TSV), SiN film with low deposition temperature of 150 °C has been developed and applied for TSV process without degradation for electrical characteristics. The uniformity of Cu electro-plating has been improved that the overburdened Cu from the surface was decreased from 13.3 μm to 0.7 μm by optimizing plating solution. The CMP process following Cu electro-plating has been customized for the high rate of 5 μm/min. Finally, the stacked wafer has been evaluated for thermal cycle test (TCT) of 100 cycles with -65 to 150 °C. The result showed that there was no degradation for packaging process.

Introduction
Although there are various methods reported for three dimensional integration (3DI) of semiconductor devices, the production cost remains as a big issue. Therefore, it is necessary to use not the state-of-the art technology but the conventional facilities and technology. In addition, the production yield must be so high that technological difficulty for production processes has to be set as low as possible.

In order to reduce the issues shown above, the aspect ratio of TSV has to be as small as possible. In this paper, the thickness of stack-wafer was thinned down to less than 10 μm. The thinned wafer was stacked on a base wafer with an adhesive polymer following TSV formation with Cu filling for interconnection. The TSV was formed by Deep Reactive Ion Etching (DRIE) process and the via diameter was 10 μm. The aspect ratio of the TSV was just 1.5 that was not difficult for production. The side-wall dielectric film was deposited and formed by PE-CVD and RIE respectively. The Cu filling and re-distribution layer (RDL) were formed simultaneously by damascene process. This TSV formation process was very close to BEOL process, which contributed to both production cost and yield. We call the process “Wafer-on-Wafer (WOW)”. By repeating the WOW process, multi-wafer-stack was finally achieved, which lead to realize high-density 3D integration with production worthy process [1-3].

The key technologies for WOW process were categorized into four parts; 1) wafer-thinning, 2) wafer stacking [4], 3) TSV formation with Cu filling [5-6], and 4) packaging. In case of the wafer thinning, the impact of the thinning process on CMOS logic device has been confirmed by the wafer thickness down to less than 10 μm. It was resulted that the wafer thinning of 10 μm was not significantly influenced on the devices, described in [3, 7]. All the process has been carried out with 8 inch wafer.

Process Flow
Figure 1 shows the process flow for WOW. A silicon wafer was deposited SiO of 1 μm by PE-CVD (Plasma Enhanced Chemical Vapor Deposition) on the multi-layer of LP-CVD (Low Pressure Chemical Vapor Deposition) SiN (200nm)/ thermal SiO (500 nm). The SiO of 1 μm was etched by RIE with the pattern of RDL (Re-Distribution Layer). The silicon wafer was temporarily bonded on a support glass wafer with an adhesive polymer. After the bonding, back side of the silicon wafer was ground down to 10 μm thick.

Following the back-grind process, the thinned wafer was bonded on a base silicon wafer with a permanent adhesive of 5 μm. The bonding material was CYCLOTENE™ (DVS-BCB). The bonding was performed with top to bottom alignment. The base silicon wafer had been patterned with Cu pads on SiN/SiO2 dielectric layers before the bonding. The Cu pads were created by single damascene process. After the seed/barrier layer of Cu/TiN/Ti was deposited by sputtering on the SiO layer that had been etched by RIE, Cu was deposited by electroplating. Then, the Cu pads were processed by CMP. The thickness of these layers was 1 μm for Cu, 50 nm for TiN and Ti. After the bonding process with the permanent adhesive, the support glass wafer was separated and the silicon wafer was cleaned with the remover solution for the temporary bonding.

For TSV creation, photo-resist was patterned on the thinned wafer stacked on the base wafer. The TSVs were etched by Deep Reactive Ion Etching (DRIE) shown in Figure 2 with small scallops of 100 nm P-V. The diameter of the TSV holes was 10 μm. After the BCB layer was etched by RIE with oxygen plasma, a dielectric layer of SiN with 500nm thickness was deposited by PE-CVD. The SiN layer was etched by anisotropic RIE without any masks, remaining the dielectric layer on the side wall and removing the top and the bottom, as shown in Figure 3. Following the sputtering of a
seed/barrier layer (Cu: 200nm, TiN: 50nm, Ti: 50nm), the TSVs were filled with Cu by electro-plating. The top of Cu on TSVs was flattened by CMP. The metallization process was almost similar to dual damascene process of BEOL. By repeating the processes shown above, thinned wafers were stacked on one by one, which enabled us to realize high density 3-D stacking.

Figure 1. Process Flow

A. Back Grind

B. BCB Bonding

C. TSV Etching

D. Side-wall Dielectric film

E. Cu Electro-plating & CMP

Figure 3. Side wall Dielectrics (SiN)

Stacking Technology in wafer-level

For the wafer-level stacking process, the thinned wafer was stacked on a base wafer with the adhesive polymer of CYCLOTENE™. The wafer was stacked with the quality of voids less than a few μm size and its alignment error of less than 5 μm on 200mm wafer-level, controlling pre-cure temperature as shown in Figure 4.

Figure 4. Alignment/Voids optimization

The thickness variation of a silicon wafer after back-grinding was also measured optically. After the silicon wafer was thinned down to 10 μm, the TTV was 6.4 μm initially as shown in Figure 5. The TTV of the silicon wafer was almost corresponded to that of the temporary adhesive. By taking into consideration of the following process, RIE, DRIE, CMP and so on, the TTV of the thinned wafer must be minimized as small as possible. It is necessary to improve the uniformity of the temporary adhesive polymer in the bonding process. The bonding process was optimized in several points of the bonding conditions, for instance, coating uniformity, pressure plate for bonding, bonding temperature, and so on. Finally, it was achieved that the TTVs of the adhesive and the silicon wafer were improved to 1.1 and 1.2μm, respectively shown in Figure 5.
TSV formation technology

Another point for the TSV formation was side-wall dielectric film. SiN film was deposited by PE-CVD at the low temperature of 150 °C. The barrier characteristics of the film were analyzed by SIMS depth profile with parameter of deposition temperature (Figure 6) and leakage current measurement. It was evaluated that the side-wall dielectric film of SiN deposited at 150 °C enabled as barrier layer of Cu diffusion for TSV.

In the TSV formation, the Cu damascene process for WOW was the most important. After the Cu was filled in the via by electroplating, CMP process which was customized for high speed rate of 5μm/min with improvement of slurry was carried out. It was shown that the Damascene process was applicable even on the surface of the thinned wafer with 10 μm thick stacked on the base silicon wafer. The uniformity of Cu electro-plating has also improved. The overburdened Cu from the surface was reduced from 13.3 μm to 0.7 μm by optimizing plating solution, as shown in Figure 7. In addition, voids in TSVs were also controlled by optimizing plating solution.

After all the processes have been optimized, the reliability of TSV interconnect has been evaluated. The thinned wafer of 10 μm thick was stacked on the wafer of 45 nm Node BEOL interconnects following thermal test of 1000 cycles. There was no resistance change in the Cu interconnects with TSVs. Leakage current between TSVs and Si substrate was low as well as 2.3 x 10⁻¹¹ A. After 1000 cycles of TC testing from -55 °C to 125 °C, resistance through TSV and Cu interconnects was not changed.

Packaging Evaluation

The impact of packaging with the WOW process has been confirmed by molding the stacked chips. After the thinned wafer was stacked on the base wafer, the wafer was diced into chips. Then, the chips were packaged by molding. The impact of molding process was evaluated by Scanning Acoustic Tomography (SAT) observation. There was no degradation after molding process. Then, thermal cycle test has been performed for the stacked chip with molding. The thermal cycles were 10² times with alternation of temperature from -65 °C to 150 °C. There was also no degradation after the thermal stress test as shown in Figure 8.

Conclusions

The WOW technology has been developed for realizing high-yield and production worthy process. The TTV for the wafer-level stacking was
optimized for 1.2μm. The low temperature deposition of 150 °C by PE-CVD has been developed and evaluated by SIMS and electrical leakage measurement. For Cu electro-plating, the plating solution has been improved, leading without void and decrease of the overburden Cu thickness from 13.3 to 0.7μm. The interconnection of TSVs filled with Cu has also confirmed and shown that resistance through TSV and Cu interconnects was not changed. The impact of packaging has been observed that there was no degradation after molding process and thermal cycle test. Finally, it was shown that the WOW process was applicable and product-worthy for the 3DI.

Acknowledgments

This work is carried out at 3D development program in the WOW alliance and the WOW Research Center Corporation. We would like to thank DISCO Corporation and Nissan Chemical for wafer thinning, bonding.

References