1. Introduction

Three-dimensional (3D) approaches have been proposed on the basis of next-generation 2D transistors and 3D architectures, and recent attention has focused on productivity and the costs involved in volume production. Stacking at the wafer level drastically increases the processing throughput, and multiple bumpless Through Silicon Vias (TSVs) provide a yield equivalent to or greater than 2D scaling beyond 22 nm nodes. Also, since this approach is compatible with existing wafer processing facilities, transistors with three-dimensional structures can be designed in a continuous manufacturing line.

This paper describes trends in conventional scaling compared with advanced technologies such as 3D integration (3DI) and bumpless TSV processes.

2. Bumpless Multi-TSV using Damascene Process

The key features in bumpless TSVs as a second-generation alternative to the use of micro-bump and Wafer-on-Wafer (WOW) technologies are the fabrication of three-dimensional structures in which any number of thinned 300 mm wafers can be stacked back-to-front and self-aligning multi-TSV interconnects without bumps as shown in Figure 1. WOW is the third-generation replacement for Chip-on-Chip (COC) technology and is also applicable to bumpless wafer-based Chip-on-Wafer (COW). Stacking at the wafer level drastically increases the processing throughput, and bumpless multi-TSVs provide a yield equivalent to or greater than that achievable with 2D scaling beyond 22 nm nodes. Also, since it is compatible with existing wafer processing facilities, transistors with three-dimensional structures can be designed in a continuous manufacturing line.

3. Thinned Wafer-on-Wafer Technology

WOW is classified into two types, according to the stacking method: Thinning before Bonding and Via-Last after Bonding. The development of WOW has proceeded through four modules, classified along the process flow. The modules include a thinning module for thinning the wafer substrates in which devices are implemented, a stacking module for bonding and stacking the wafers, a TSV interconnects module for forming Cu interconnects embedded in upper and lower wafers with TSVs, and a packaging module for singulating the stacked wafers as shown in Figure 2.

4. TSV Module

For TSV processing and embedded interconnects, including redistribution, the Damascene method is employed to simplify the processes as shown in Figure 3. For TSV processing, the Bosch method, involving alternately repeating etching and redeposition of protective films, is used. The TSV etching profile and process time vary greatly depending on the TSV depth and aspect ratio. With WOW technology, the aspect ratio can be reduced because TSVs are formed in pre-thinned wafers. For this reason, conventional dry etching can also be used, and the time required for the etching and embedded interconnects processes can be reduced, thus allowing enhanced productivity.

To provide electrical insulation from Si, which is a conductor, a plasma-enhanced chemical-vapor-deposition Silicon-oxy-nitride (PECVD-SiON) film is deposited after TSV processing. The film density of the PECVD-SiON film decreases with deposition temperature—the density is reduced to half at 150 °C—and the composition becomes incompatible with the stoichiometry, degrading the diffusion barrier characteristics. However, effective barrier characteristics can be achieved with sufficient film thicknesses of around 100 nm. This is an advantage specific to large TSVs, unlike via-holes in the Cu/low-k process that requires barrier characteristics at an extreme thickness, such as 10 nm. The SiON film at the bottom of the WOW is removed by bias sputtering, and Ti/TiN and Cu are deposited on the barrier metal and the seed layer, respectively, by sputtering. For Cu embedded interconnects, electrochemical deposited Cu (ECD-Cu) is used. ECD-Cu planarization is carried out by chemical mechanical polishing (CMP).

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